## TP44100SG-TPPFC520-EVB

### 520 W Totem-Pole PFC Evaluation Board Using Tagore Technology's Superior GaN HEMT (TP44100SG)

### User Manual

### Rev-1.0

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#### **About this document**

#### **Objective and Purpose:**

This application note describes Tagore Technology's 520 W Totem-Pole PFC (TP-PFC) Converter Evaluation Board (TP44100SG-TPPFC520-EVB) using its 90 mΩ superior GaN HEMT TP44100SG. The user will be able to perform a complete evaluation of the EVB by following the procedures outlined in this document and all the necessary supporting information (circuit schematics, BOM, layout, key operating waveforms, etc.) is provided to facilitate a quick adaption to a production design.

#### **Intended audience:**

This application note is intended for Tagore Technology's customers and partners using its 90 mΩ Superior GaN HEMT TP44100SG.

#### **Revision History**



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#### **Contents**





#### <span id="page-3-0"></span>**1 Introduction**

In most of the power supplies and battery chargers connected to grid, ac-dc power conversion serves as the first-stage power conversion block. Above 75 W output power, regulations require incorporation of a Power Factor Correction (PFC) stage in the ac-dc converter.

The **TP44100SG-TPPFC520-EVB** is a highly efficient single phase Totem Pole PFC (TP-PFC) solution, which is built using the advantages of Tagore Technology's Superior GaN HEMT **TP44100SG**. The EVB can operate over the universal input ac voltage range (90 V to 265 V) providing output power up to 520 W with efficiency more than 98%. Such high efficiency cannot be achieved using a standard Boost PFC due to high power loss in the Diode Bridge Rectifier (DBR) at its input. The Totem Pole PFC topology replaces the inefficient diodes bridge with semiconductor switches. Tagore Technology's "Enhancement Mode High Electron Mobility GaN Transistors (E-HEMTs) with ESD protection" parts have very low output charge ( $Q<sub>oss</sub>$ ), while the reverse recovery charge ( $Q<sub>rr</sub>$ ) is completely absent. These advantages of Tagore Technology's Superior GaN part **TP44100SG** are leveraged here to design this TP-PFC solution with low switching loss and enhanced efficiency.



**Figure 1-1: Photograph of TP44100SG-TPPFC520-EVB.**

Lower device loss allows the GaN HEMTs to operate continuously without any need for external heatsink. This significantly helps reduce the volume and weight of the EVB. The TP44100SG parts are Surface Mount Devices (SMDs) that come in small QFN 5x7 package. This further enables a very compact PCB layout design and helps improve the EMI performances of the converter by controlling the switching voltage oscillations. Utilizing these advantages, the TP-PFC solution has been designed to have a small form factor, and hence, high power density. Additional thermal management like fan and heatsink are not required. The use of SMD components makes the assembly process faster and cheaper. Thus, this TP-PFC solution using Tagore Technology's Superior GaN is an ideal candidate for a simple, compact, and cost-effective PFC application.

#### <span id="page-3-1"></span>**1.1 Working Principle**

The TP-PFC has four switching devices, distributed in two switching legs. The two High Frequency (HF) GaN HEMT, S1 and S2, and two Low Frequency (LF) Super-Junction (SJ) MOSFETs, S3 and S4 as shown in [Figure 1-2.](#page-4-0) The LF devices are turned ON and OFF alternately in each line cycle. This divides



the TP-PFC into two different functional boost converters with synchronous rectification. The HF leg GaN HEMTs change their role between boost switch and boost diode every half line cycle. During the positive half line cycle, the LF MOSFET S4 is turned ON and S3 is turned OFF. Here, the GaN HEMT S2 acts as the boost switch, driven with duty cycle D, and S1 acts as the boost diode, driven with complementary PWM signal of duty (1-D). Similarly, during the negative half line cycle, S3 remains ON and SRL OFF. The GaN HEMT S2 acts as the boost diode and S1 as the boost switch.



**Figure 1-2: Functional block diagram of EVB.**

<span id="page-4-0"></span>The NCP1680 is a Critical Conduction Mode (CrM) PFC controller IC dedicated for TP-PFC topology. In a switching cycle, when the boost switch is turned on, the inductor current rises in magnitude. After the boost switch is turned off, this inductor current gradually returns to zero as the output capacitor gets charged. The controller needs to detect the exact instant when the inductor current just falls to zero so that it can initiate the next switching cycle as per the CrM operating mode. This is achieved through negative dc bus current sensing (ZCD sense through the current sense resistor  $R_{\rm sns}$ ) as shown in Figure [1-2.](#page-4-0) The TP-PFC also operates at DCM at light loads, and during some part of the line cycle to prevent the switching frequency going very high. During this time, the boost GaN switches are turned on at the Quasi Resonant (QR) valleys of switching node voltage to reduce the turn on switching losses and to improve the EMI performance. The switch node valleys are being sensed using an auxiliary winding, coupled to the boost inductor, and the information is fed to the controller IC as shown in [Figure 1-2.](#page-4-0) Three resistor potential divider networks are used: The first two for sensing the line voltage (not shown here), and the rest for output dc bus voltage sense as shown by the resistors R1 and R2.

The controller IC does not have integrated gate drivers to drive the semiconductor switches. So, external half-bridge level-shifted gate driver ICs (NCP 51530) are required to drive both the HF and LF legs of the TP-PFC converter (shown in the schematic). These gate drivers take PWM signals from the controller IC as inputs and generate gate drive output pulses of 12 V as high level and 0 V as low level. Since the GaN HEMTs need +6V/0V gate drive signals, interface circuit/level-down-shifter circuit has been used between the gate terminal of each GaN HEMT and its respective gate driver output. The detailed interface circuit is illustrated in [Figure 1-3.](#page-5-0)



**Figure 1-3: Gate Interface Circuit.**

<span id="page-5-0"></span>The controller does not have self-startup functionality. It needs external bias supply for startup and run. The entire control circuit, including gate drivers, has been designed to work with 12  $V_{dc}$  supply. An auxiliary power supply daughter board is used. It takes power from the output dc bus (~400 V) and provides 12  $V_{dc}$  to the controller circuit. During startup, the output dc bus capacitor initially gets peak charged to the peak of the line voltage through the body diodes of the LF MOSFETs S3 and S4, and the bypass diodes (shown in the schematic) to provide the initial bias power. The bias power supply has been designed to operate from very low voltage ( $\sim$ 50 V<sub>dc</sub>) to maximum possible dc bus voltage ( $\sim$ 400 V).

At input voltages below 180  $V_{ac}$ , the output power should be derated to 240 W. So, the user should be careful to connect proper load depending on the input ac supply voltage conditions.



**Figure 1-4: Recommended derating of maximum output power vs input ac voltage at 25° C or less.**



#### <span id="page-6-0"></span>**2 Physical Details and Specifications Of EVB**

Photographs of both the top and the bottom sides of the TP-PFC EVB are shown in [Figure 2-1](#page-6-3) with key components identified.



**Top Side** 

**Bottom Side** 

**Figure 2-1: Top (Left) and Bottom (Right) views of the EVB with key circuit blocks identified.**

#### <span id="page-6-3"></span><span id="page-6-1"></span>**2.1 Dimension Measurements**

#### **Table 2-1 : Mechanical Dimensions**



#### <span id="page-6-2"></span>**2.2 Technical Data**





 $*$  At input voltages below 180  $V_{ac}$ , the maximum output power should be derated to 240 W.

#### <span id="page-7-0"></span>**3 Operating Procedure**

#### <span id="page-7-1"></span>**3.1 List Of Instruments and Hardware Items Required**

For testing the Eval Board, following list of instruments and hardware items are required:

- TP44100SG-TPPFC520-EVB
- AC Power Source: Output voltage within 90  $V_{ac}$  to 265  $V_{ac}$ ; capable of delivering 250 W power.
- Load: Electronic Load or Resistive Load  $(400 V_{dc}$  min., 520 W)
- Observation Instruments:
	- Digital Power Meter GWInstek GPM-8213 or equivalent
	- **•** Digital Multimeters for measuring voltages and currents (300  $V_{ac}$  min., 5 A min.)
	- Digital Storage Oscilloscope (DSO) (Preferably with 4 Channels, BW ≥ 300 MHz)
	- **EXECT** High Voltage Differential Probes (min. 500 V) compatible with the DSO
	- Current Clamp Probes (min. 10 A) compatible with the DSO
- Wires and cables for making electrical connections.

#### <span id="page-7-2"></span>**3.2 Operating Procedure Steps**

- Ensure that the dc bus capacitors are discharged, the output voltage of EVB is zero, and the ac power source is turned off.
- Connect the input power terminals of the EVB to the output terminals of the ac power source. (Optional: Connect a power meter in between the EVB input and ac power source output).
- Set electronic load value to 0A in constant current mode and ensure loading is disabled. Connect the output terminals of the EVB to the electronic load in correct polarity.
- Connect voltage, current probes from DSO to the desired observation points.
- Set the output of the ac power source to 0 Vac and then switch it on. Gradually increase the ac output to 90 Vac. Observe that the EVB output voltage will rise to ~400 Vdc and maintain the same value indicating that the EVB startup is complete.
- Enable the electronic load and then gradually increase the loading to the desired value not exceeding the maximum output power rating of the EVB while doing these experiments. At input voltage below 180 Vac adhere to the recommended derating of the maximum output power.
- After completing experiments, turn off the ac input power source. Wait for some more time for the output dc bus to get discharged before touching the board.



#### <span id="page-8-0"></span>**4 Experimental Results**

#### <span id="page-8-1"></span>**4.1 Efficiency**

Efficiency measurement test is done by measuring the input power using a digital power meter, while the output voltage and currents were measured by the electronic load. Measured efficiency of the EVB at various loads for different input voltages is shown in [Figure 4-1.](#page-8-3)



**Figure 4-1: EVB Efficiency measured at two different input voltages: 115 Vac and 230 Vac.**

#### <span id="page-8-3"></span><span id="page-8-2"></span>**4.2 Power Factor**

Power factor curves vs output power at different input voltages are shown in [Figure 4-2.](#page-8-4)



<span id="page-8-4"></span>**Figure 4-2: Power Factor vs Output Power at 115 Vac and 230 Vac.**

#### <span id="page-9-0"></span>**4.3 Steady-State Input Waveforms**

Typical steady state input voltage and current waveforms of the EVB for different cases:

- Input Voltage: 180 V<sub>ac</sub> and Output Power: 520 W is shown in [Figure 4-3.](#page-9-1)
- Input Voltage: 230  $V_{ac}$  and Output Power: 520 W is shown in [Figure 4-4.](#page-9-2)
- Input Voltage:  $230 \text{ V}_{ac}$  and Output Power: 240 W is shown in [Figure 4-5.](#page-10-0)
- Input Voltage: 115  $V_{ac}$  and Output Power: 240 W is shown in [Figure 4-6.](#page-10-1)



<span id="page-9-1"></span>**Figure 4-3: Input voltage and current waveforms at 520 W load and 180 Vac input. Channel 1(Blue): Input voltage (100 V/div.); Channel 2(Red): Input current (5 A/div.); time: 5 ms/div.**



<span id="page-9-2"></span>**Figure 4-4: Input voltage and current waveforms at 520 W load and 230 Vac input. Channel 1(Blue): Input voltage (100 V/div.); Channel 2(Red): Input current (5 A/div.); time: 5 ms/div.**



<span id="page-10-0"></span>**Figure 4-5: Input voltage and current waveforms at 240 W load and 230 Vac input. Channel 1(Blue): Input voltage (100 V/div.); Channel 2(Red): Input current (5 A/div.); time: 5 ms/div.**



<span id="page-10-1"></span>**Figure 4-6: Input voltage and current waveforms at 240 W load and 115 Vac input. Channel 1(Blue): Input voltage (100 V/div.); Channel 2(Red): Input current (5 A/div.); time: 5 ms/div.**

THD of the input current at two input voltages 230  $V_{ac}$  and 115  $V_{ac}$  for different loads are given in the table below:







#### <span id="page-11-0"></span>**4.4 Start-up**

The EVB is designed to limit the initial inrush current at the input during start-up. The output voltage gradually builds up from the peak of the line voltage to its final reference value without having any overshoot. The no load start-up waveforms of the EVB at 115 Vac and 230 Vac are shown in [Figure 4-7](#page-11-1) and [Figure 4-8](#page-11-2) respectively. These indicate that the start-up procedure is completed in less than 0.5 s.



<span id="page-11-1"></span>**Figure 4-7: No-load start-up at 115 Vac input. Channel 1(Blue): Input ac voltage (200 V/div); Channel 2(Red): Input ac current (5 A/div); Channel 3(Green): TP-PFC high frequency leg switch node voltage (200 V/div); Channel 4(Orange): Output voltage (200 V/div); time: 50 ms/div.**



<span id="page-11-2"></span>**Figure 4-8: No-load start-up at 230 Vac input. Channel 1(Blue): Input ac voltage (500 V/div); Channel 2(Red): Input ac current (5 A/div); Channel 3(Green): TP-PFC high frequency leg switch node voltage (200 V/div); Channel 4(Orange): Output voltage (200 V/div); time: 50 ms/div.**

#### <span id="page-12-0"></span>**4.5 Load Step Change Transient Response**

The TP-PFC EVB has been designed to have fast load dynamic response. Output voltage responses to a step change in load between 0 - 240 W and vice-versa are shown in [Figure 4-9](#page-12-1) and [Figure 4-10](#page-12-2) respectively, for both 115 V<sub>ac</sub> and 230 V<sub>ac</sub> input voltages. Voltage undershoots and overshoots are less than 0.8% of the nominal output voltage. It should be noted that the noise signal around the load current waveforms (Red) is due to current probe pickup noise, which is not present in the actual current.



<span id="page-12-1"></span>**Figure 4-9: PFC output voltage transient due to 0-240 W load step change at (Left) 115 Vac and (Right) 230 Vac. Channel 1 (Blue): Output voltage (10 V/div); Channel 2(Red): Output load current (1 A/div); time: 50 ms/div.**



<span id="page-12-2"></span>**Figure 4-10: PFC output voltage transient due to 240-0 W load step change at (Left) 115 Vac and (Right) 230 Vac. Channel 1 (Blue): Output Voltage (10 V/div); Channel 2(Red): Output Load current (1 A/div); time: 50 ms/div.**



#### <span id="page-13-0"></span>**4.6 Output Voltage Ripple Switching Waveforms**

Output voltage ripple waveform at 240 W and 115  $V_{ac}$ , and at 520 W and 230  $V_{ac}$  are shown in Figure [4-11.](#page-13-2) The measured peak-to-peak ripple is less than 20 V.



<span id="page-13-2"></span>**Figure 4-11: Output voltage ripple waveforms on full load at (Left) 115 Vac and (Right) 230 Vac. Channel 1(Blue): Output voltage ripple (10 V/div.); Channel 2(Red): Output Load current (0.5 A/div.).**

#### <span id="page-13-1"></span>**4.7 Switching Waveforms**

The high frequency switch node voltage and the corresponding Gate-Source voltage waveform of the Low side GaN HEMT S2 of the high frequency leg of the TP-PFC are shown in [Figure 4-12.](#page-13-3)



<span id="page-13-3"></span>**Figure 4-12: Channel 1(Blue): High Frequency switch node voltage (100 V/div.); Channel 2(Red): Gate-Source voltage of the Low side GaN FET (10 V/div.); Channel 3(Green): Input current (2 A/div.); (Above) Waveforms captured over few line cycles, (Below) zoomed to 5 μs/div.**



#### <span id="page-14-0"></span>**4.8 Thermal Performance**

The thermal performance of the GaN HEMTs is captured at 230  $V_{ac}$  and 115  $V_{ac}$  input voltages and maximum output power of 520 W and 240 W, respectively. The thermal images are shown in [Figure 4-13.](#page-14-2) It shows that there is a temperature rise of 31  $\degree$  over the ambient temperature of 25 $\degree$ C.



<span id="page-14-2"></span>**Figure 4-13: Temperature measurement of GaN HEMTs at 520 W, 230 Vac (Left) and 240 W, 115 Vac (Right).**

#### <span id="page-14-1"></span>**5 PCB Layout**

This section presents the PCB layout for the different layers of the main 4-layer power board.



**Figure 5-1: Top layer.** The state of the state of the Figure 5-2: Mid layer 1

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**Figure 5-3: Mid layer 2. Figure 5-4: Bottom layer.**

#### <span id="page-15-0"></span>**Bill Of Materials**

#### **Table 6-1: Bill of Materials (BOM)**



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#### <span id="page-17-0"></span>**7 Schematic Diagram**

The electrical schematic diagram of the EVB is provided in this section.





